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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
IWASHKO, LEV	
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2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,137	BRADLEY ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because Figures 1-6 are hand-written. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-7, 9-12, 14-20, and 22-25 are rejected under U.S.C. 102(e) as being anticipated by Swoboda (US PGPub 2004/0117717).

Claim 1. Apparatus for processing data, said apparatus comprising:

- data processing logic operable to execute data processing operations; *(Section 0030, lines 5-7 – State the following: "When an export trace packet is available, a PACKET AVAILABLE signal is applied to logic "OR" gate 83 and to a control terminal of multiplexer 82")*
- one or more trace data sources operable to generate respective streams of trace data for said data processing logic; *(Section 0028, lines 1-8 – State the following: "Referring to FIG. 6B, the reconstruction of the program execution from the timing and program counter trace streams is illustrated. The timing trace stream consists of packets of 8 logic "0"s and logic "1"s. The logic "0"s indicate that either the program counter or the pipeline is advanced, while the logic "1"s indicate the either the program counter or the pipeline is stalled during that clock cycle")*
- one or more trace data sinks operable to receive respective streams of trace data from said one or more trace data sources; *(Section 0030, lines 1-12 – State the following: "Referring to FIG. 8, the apparatus for converting the trace packets to export trace packets is shown. Trace packets are applied to trace packets unit 81. In trace packets units 81, the trace packets are grouped into export trace packets. When an export trace packet is available, a PACKET AVAILABLE signal is applied to logic "OR" gate 83 and to a control terminal of multiplexer 82. When the PACKET AVAILABLE signal is present, an export race packet is transmitted through the multiplexer 82 and applied to export trace unit 84. From export trace unit 84, the export trace packets are transferred to the host processing unit (not shown). ")*
- and at least one flush signal generator operable to generate a flush request signal passed to at least one of said one or more trace data sources to signal a flush point within any trace data buffered within said at least one of said one or more trace data sources; wherein said at

least one of said one or more trace data sources is operable to trigger a flush complete response when any trace data generated by said at least one trace data source prior to said flush point has been output to one of said one or more trace data sinks. *(Section 0030, lines 12-23 – State the following: "When an export trace packet is received by the export trace unit 84, a PACKET ACKNOWLEDGE signal is applied to the trace packets unit 81 and the flush packet unit 86. 1-bit register 85 receives a HALT DURING A NON_INTERRUPTIBLE CODE SEGMENT signal. This signal sets a bit in 1-bit register 85. The bit in 1-bit register 85 applies a control signal to flush packet unit 86. The flush packet unit 86 has trace packets applied thereto and applies a PACKET AVAILABLE signal to a second input terminal of logic "OR" gate 83. In the presence of the control signal applied to flush packet unit 86, flush packets are applied through the multiplexer 82 to the export trace packet unit 84")*

Claim 2. Apparatus as claimed in claim 1, wherein said at least one of said one or more trace data sources continue to generate trace data following receipt of said flush request signal. *(Section 0031, lines 1-16 – State the following: "Referring to FIG. 9, the operation of the present invention is illustrated. The trace packets are generated and converted to export trace packets. After a halt is signaled during a non-interruptible code segment, execution of the code segment is continued until an appropriate halt point is found. The present invention, as shown in FIG. 9, stops generating trace packets. Export trace packets are generated for the trace packets that have been generated. However, when there is a remainder, the flush trace unit generates a flush packet that completes the data generated by the non-interruptible code segment. The flush packet will add logic "0"s to the incomplete packets. In addition, flush packets will be generated to provide sufficient logic signals to populate a standard memory location in the memory unit. When the target processor begins operation after a*

pause, the trace packets are converted into export trace packets as before")

Claim 3. Apparatus as claimed in claim 1, wherein said flush complete response comprises generating a flush complete signal passed to said at least one flush signal generator. *(Section 0033, lines 10-11 – State the following: "Logic "0"s complete the contents of the flush packets")*

Claim 4. Apparatus as claimed in claim 3, wherein said at least one flush signal generator passes said flush request signal to a plurality of trace data sources and receipt of flush complete signals from all of said plurality of trace data sources indicates all trace data generated by said plurality of trace data source prior to said flush point has been output. *(Section 0033, lines 11-14 and Section 0034, lines 1-14 – State the following:. "In addition, flush packets are generated to insure that logic signals are available to populate the memory locations into which the packet group payloads are being entered. The present invention relies on the ability of relate the timing trace stream and the program counter trace stream. This relationship is provided by having periodic sync ID information transmitted in each trace stream. In addition, the timing packets are grouped in packets of eight signals identifying whether the program counter or the pipeline advanced or didn't advance. The sync markers in the program counter stream include both the periodic sync ID and the position in the current eight position packet when the event occurred. Thus, the clock cycle of the event can be specified. In addition, the address of the program counter is provided in the program counter sync markers so that the debug halt event can be related to the execution of the program".)*

Claim 5. Apparatus as claimed in claim 1, wherein said at least one flush signal generator is part of a trace data sink. *(Section 0030, lines 1-12 – State the following: "Referring to FIG. 8, the apparatus for converting the trace packets to export trace packets is shown. Trace packets are applied to*

trace packets unit 81. In trace packets units 81, the trace packets are grouped into export trace packets. When an export trace packet is available, a PACKET AVAILABLE signal is applied to logic "OR" gate 83 and to a control terminal of multiplexer 82. When the PACKET AVAILABLE signal is present, an export race packet is transmitted through the multiplexer 82 and applied to export trace unit 84. From export trace unit 84, the export trace packets are transferred to the host processing unit (not shown). State the following: "When an export trace packet is received by the export trace unit 84, a PACKET ACKNOWLEDGE signal is applied to the trace packets unit 81 and the flush packet unit 86. 1-bit register 85 receives a HALT DURING A NON_INTERRUPTIBLE CODE SEGMENT signal. This signal sets a bit in 1-bit register 85. The bit in 1-bit register 85 applies a control signal to flush packet unit 86. The flush packet unit 86 has trace packets applied thereto and applies a PACKET AVAILABLE signal to a second input terminal of logic "OR" gate 83. In the presence of the control signal applied to flush packet unit 86, flush packets are applied through the multiplexer 82 to the export trace packet unit 84")

Claim 6. Apparatus as claimed in claim 1, wherein one or more trace data buses connect said one or more trace data sources to said one or more trace data sinks and at least one bus bridge is interposed within one of said one or more trace data buses, said at least one flush signal generator being part of one of said at least one bus bridge. *(Figure 2 – Shows buses that lead to the trace data generator. Section 0029, lines 1-25 – State the following: "Referring to FIG. 7, the general technique for reconstruction of the trace streams is illustrated. The trace streams originate in the target processor 12 as the target processor 12 is executing a program 1201. The trace signals are applied to the host processing unit 10. The host processing unit 10 also includes the same program 1201. Therefore, in the illustrative example of FIG. 6 wherein the program execution proceeds*

without interruptions or changes, only the first and the final absolute addresses of the program counter are needed. Using the advance/non-advance signals of the timing trace stream, the host processing unit can reconstruct the program as a function of clock cycle. Therefore, without the sync ID packets, only the first and last sync markers are needed for the trace stream. This technique results in reduced information transfer. FIG. 6 includes the presence of periodic sync ID cycles, of which only one is shown. The periodic sync ID packets are important for synchronizing the plurality of trace streams, for selection of a particular portion of the program to analyze, and for restarting a program execution analysis for a situation wherein at least a portion of the data in the trace data stream is lost. The host processor can discard the (incomplete) trace data information between two sync ID packets and proceed with the analysis of the program outside of the sync timing packets defining the lost data")

Claim 7. Apparatus as claimed in claim 6, wherein said at least one bus bridge is a power-down bus bridge operable upon receipt of a power-down signal to generate a flush request signal *(Section 0031, lines 1-16 – State the following: "Referring to FIG. 9, the operation of the present invention is illustrated. The trace packets are generated and converted to export trace packets. After a halt is signaled during a non-interruptible code segment, execution of the code segment is continued until an appropriate halt point is found. The present invention, as shown in FIG. 9, stops generating trace packets. Export trace packets are generated for the trace packets that have been generated. However, when there is a remainder, the flush trace unit generates a flush packet that completes the data generated by the non-interruptible code segment. The flush packet will add logic "0"s to the incomplete packets. In addition, flush packets will be generated to provide sufficient logic signals to populate a standard memory location in the memory unit. When the target processor begins operation after a*

pause, the trace packets are converted into export trace packets as before")

- and to delay power down of said one or more trace data sources until all trace data generated by said trace data sources prior to said flush point has been output. *(Section 0033, lines 1-3 – State the following: "The present invention provides a technique for completing the transfer of trace data after the generation of halt signal for a non-interruptible code segment")*

Claim 9. Apparatus as claimed in claim 7, wherein said data processing logic for which said one or more trace data sources generates trace data is powered down with said one or more trace data sources. *(Section 0033, lines 10-14 – State the following: "Logic "0"s complete the contents of the flush packets. In addition, flush packets are generated to insure that logic signals are available to populate the memory locations into which the packet group payloads are being entered")*

Claim 10. Apparatus as claimed in claim 9, wherein said data processing logic and said one or more trace data sources are within a common power domain within an integrated circuit comprising a plurality of power domains. *(Section 0034, lines 1-14 – State the following, which denotes a plurality of power domains as each stream can be turned off individually. The present invention relies on the ability of relate the timing trace stream and the program counter trace stream. This relationship is provided by having periodic sync ID information transmitted in each trace stream. In addition, the timing packets are grouped in packets of eight signals identifying whether the program counter or the pipeline advanced or didn't advance. The sync markers in the program counter stream include both the periodic sync ID and the position in the current eight position packet when the event occurred. Thus, the clock cycle of the event can be specified. In addition, the address of the program counter is provided in*

the program counter sync markers so that the debug halt event can be related to the execution of the program")

Claim 11. Apparatus as claimed in claim 1, wherein said flush signal generator operable upon receipt of a power-down signal to generate and flush request signal and to delay power down of said one or more trace data sources until all trace data generated by said trace data sources prior to said flush point has been output. *(Section 0031, lines 1-16 – State the following: "Referring to FIG. 9, the operation of the present invention is illustrated. The trace packets are generated and converted to export trace packets. After a halt is signaled during a non-interruptible code segment, execution of the code segment is continued until an appropriate halt point is found. The present invention, as shown in FIG. 9, stops generating trace packets. Export trace packets are generated for the trace packets that have been generated. However, when there is a remainder, the flush trace unit generates a flush packet that completes the data generated by the non-interruptible code segment. The flush packet will add logic "0"s to the incomplete packets. In addition, flush packets will be generated to provide sufficient logic signals to populate a standard memory location in the memory unit. When the target processor begins operation after a pause, the trace packets are converted into export trace packets as before." Section 0033, lines 1-3 – State the following: "The present invention provides a technique for completing the transfer of trace data after the generation of halt signal for a non-interruptible code segment")*

Claim 12. Apparatus as claimed in claim 6, comprising a trace data funnel operable to combine trace data signals received from a plurality of trace data sources via respective trace data buses onto a single trace data bus. *(Sections 0023-0024 – State the following: "Referring to FIG. 3, the relationship between selected components in the target processor 20 is illustrated. The data trace generation unit 201 includes a packet assembly unit 2011 and a FIFO (first in/first out) storage unit 2012, the program*

counter trace generation unit 202 includes a packet assembly unit 2021 and a FIFO storage unit 2022, and the timing trace generation unit 203 includes a packet generation unit 2031 and a FIFO storage unit 2032. As the signals are applied to the packet generators 201, 202, and 203, the signals are assembled into packets of information. The packets in the preferred embodiment are 10 bits in width. Packets are assembled in the packet assembly units in response to input signals and transferred to the associated FIFO unit. The scheduler/multiplexer 204 generates a signal to a selected trace generation unit and the contents of the associated FIFO storage unit are transferred to the scheduler/multiplexer 204 for transfer to the emulation unit. Also illustrated in FIG. 3 is the sync ID generation unit 207. The sync ID generation unit 207 applies an SYNC ID signal to the packet assembly unit of each trace generation unit. The periodic signal, a counter signal in the preferred embodiment, is included in a current packet and transferred to the associated FIFO unit. The packet resulting from the SYNC ID signal in each trace is transferred to the emulation unit and then to the host processing unit. In the host processing unit, the same count in each trace stream indicates that the point at which the trace streams are synchronized. In addition, the packet assembly unit 2031 of the timing trace generation unit 203 applies and INDEX signal to the packet assembly unit 2021 of the program counter trace generation unit 202. The function of the INDEX signal will be described below. Referring to FIG. 4A, the assembly of timing packets is illustrated. The signals applied to the timing trace generation unit 203 are the CLOCK signals and the ADVANCE signals. The CLOCK signals are system clock signals to which the operation of the central processing unit 200 is synchronized. The ADVANCE signals indicate an activity such as a pipeline advance or program counter advance (0) or a pipeline non-advance or program counter non-advance (1). An ADVANCE or NON-ADVANCE signal occurs each clock cycle. The timing packet is

assembled so that the logic signal indicating ADVANCE or NON-ADVANCE is transmitted at the position of the concurrent CLOCK signal. These combined CLOCK/ADVANCE signals are divided into groups of 8 signals, assembled with two control bits in the packet assembly unit 2031, and transferred to the FIFO storage unit 2032")

Claim 14. A method of processing data, said method comprising the steps of:

- executing data processing operations with data processing logic; *(Section 0030, lines 5-7 – State the following: "When an export trace packet is available, a PACKET AVAILABLE signal is applied to logic "OR" gate 83 and to a control terminal of multiplexer 82")*
- generating respective streams of trace data for said data processing logic with one or more trace data sources; *(Section 0028, lines 1-8 – State the following: "Referring to FIG. 6B, the reconstruction of the program execution from the timing and program counter trace streams is illustrated. The timing trace stream consists of packets of 8 logic "0"s and logic "1"s. The logic "0"s indicate that either the program counter or the pipeline is advanced, while the logic "1"s indicate the either the program counter or the pipeline is stalled during that clock cycle")*
- receiving respective streams of trace data from said one or more trace data sources with one or more trace data sinks operable; *(Section 0030, lines 1-12 – State the following: "Referring to FIG. 8, the apparatus for converting the trace packets to export trace packets is shown. Trace packets are applied to trace packets unit 81. In trace packets units 81, the trace packets are grouped into export trace packets. When an export trace packet is available, a PACKET AVAILABLE signal is applied to logic "OR" gate 83 and to a control terminal of multiplexer 82. When the PACKET AVAILABLE signal is present, an export race packet is transmitted through the multiplexer 82 and applied to export trace unit 84. From export trace unit 84, the export*

trace packets are transferred to the host processing unit (not shown). ")

- and generating with at least one flush signal generator a flush request signal passed to at least one of said one or more trace data sources to signal a flush point within any trace data buffered within said at least one of said one or more trace data sources; wherein said at least one of said one or more trace data sources is operable to trigger a flush complete response when any trace data generated by said at least one trace data source prior to said flush point has been output to one of said one or more trace data sinks. *(Section 0030, lines 12-23 – State the following: "When an export trace packet is received by the export trace unit 84, a PACKET ACKNOWLEDGE signal is applied to the trace packets unit 81 and the flush packet unit 86. 1-bit register 85 receives a HALT DURING A NON_INTERRUPTIBLE CODE SEGMENT signal. This signal sets a bit in 1-bit register 85. The bit in 1-bit register 85 applies a control signal to flush packet unit 86. The flush packet unit 86 has trace packets applied thereto and applies a PACKET AVAILABLE signal to a second input terminal of logic "OR" gate 83. In the presence of the control signal applied to flush packet unit 86, flush packets are applied through the multiplexer 82 to the export trace packet unit 84")*

Claim 15. A method as claimed in claim 14, wherein said at least one of said one or more trace data sources continue to generate trace data following receipt of said flush request signal. *(Section 0031, lines 1-16 – State the following: "Referring to FIG. 9, the operation of the present invention is illustrated. The trace packets are generated and converted to export trace packets. After a halt is signaled during a non-interruptible code segment, execution of the code segment is continued until an appropriate halt point is found. The present invention, as shown in FIG. 9, stops generating trace packets. Export trace packets are generated for the trace packets*

that have been generated. However, when there is a remainder, the flush trace unit generates a flush packet that completes the data generated by the non-interruptible code segment. The flush packet will add logic "0"s to the incomplete packets. In addition, flush packets will be generated to provide sufficient logic signals to populate a standard memory location in the memory unit. When the target processor begins operation after a pause, the trace packets are converted into export trace packets as before")

Claim 16. A method as claimed in claim 15, wherein said flush complete response comprises generating a flush complete signal passed to said at least one flush signal generator. *(Section 0033, lines 10-11 – State the following: "Logic "0"s complete the contents of the flush packets")*

Claim 17. A method as claimed in claim 16, wherein said at least one flush signal generator passes said flush request signal to a plurality of trace data sources and receipt of flush complete signals from all of said plurality of trace data sources indicates all trace data generated by said plurality of trace data source prior to said flush point has been output. *(Section 0033, lines 11-14 and Section 0034, lines 1-14 – State the following: "In addition, flush packets are generated to insure that logic signals are available to populate the memory locations into which the packet group payloads are being entered. The present invention relies on the ability of relate the timing trace stream and the program counter trace stream. This relationship is provided by having periodic sync ID information transmitted in each trace stream. In addition, the timing packets are grouped in packets of eight signals identifying whether the program counter or the pipeline advanced or didn't advance. The sync markers in the program counter stream include both the periodic sync ID and the position in the current eight position packet when the event occurred. Thus, the clock cycle of the event can be specified. In addition, the address of the program counter is provided in the program counter sync*

markers so that the debug halt event can be related to the execution of the program".)

Claim 18. A method as claimed in claim 14, wherein said at least one flush signal generator is part of a trace data sink. *(Section 0030, lines 1-12 – State the following: "Referring to FIG. 8, the apparatus for converting the trace packets to export trace packets is shown. Trace packets are applied to trace packets unit 81. In trace packets units 81, the trace packets are grouped into export trace packets. When an export trace packet is available, a PACKET AVAILABLE signal is applied to logic "OR" gate 83 and to a control terminal of multiplexer 82. When the PACKET AVAILABLE signal is present, an export race packet is transmitted through the multiplexer 82 and applied to export trace unit 84. From export trace unit 84, the export trace packets are transferred to the host processing unit (not shown). State the following: "When an export trace packet is received by the export trace unit 84, a PACKET ACKNOWLEDGE signal is applied to the trace packets unit 81 and the flush packet unit 86. 1-bit register 85 receives a HALT DURING A NON_INTERRUPTIBLE CODE SEGMENT signal. This signal sets a bit in 1-bit register 85. The bit in 1-bit register 85 applies a control signal to flush packet unit 86. The flush packet unit 86 has trace packets applied thereto and applies a PACKET AVAILABLE signal to a second input terminal of logic "OR" gate 83. In the presence of the control signal applied to flush packet unit 86, flush packets are applied through the multiplexer 82 to the export trace packet unit 84")*

Claim 19. A method as claimed in claim 14, wherein one or more trace data buses connect said one or more trace data sources to said one or more trace data sinks and at least one bus bridge is interposed within one of said one or more trace data buses, said at least one flush signal generator being part of one of said at least one bus bridge. *(Figure 2 – Shows buses that lead to the trace data generator. Section 0029, lines 1-25 – State the following:*

"Referring to FIG. 7, the general technique for reconstruction of the trace streams is illustrated. The trace streams originate in the target processor 12 as the target processor 12 is executing a program 1201. The trace signals are applied to the host processing unit 10. The host processing unit 10 also includes the same program 1201. Therefore, in the illustrative example of FIG. 6 wherein the program execution proceeds without interruptions or changes, only the first and the final absolute addresses of the program counter are needed. Using the advance/non-advance signals of the timing trace stream, the host processing unit can reconstruct the program as a function of clock cycle. Therefore, without the sync ID packets, only the first and last sync markers are needed for the trace stream. This technique results in reduced information transfer. FIG. 6 includes the presence of periodic sync ID cycles, of which only one is shown. The periodic sync ID packets are important for synchronizing the plurality of trace streams, for selection of a particular portion of the program to analyze, and for restarting a program execution analysis for a situation wherein at least a portion of the data in the trace data stream is lost. The host processor can discard the (incomplete) trace data information between two sync ID packets and proceed with the analysis of the program outside of the sync timing packets defining the lost data")

Claim 20. A method as claimed in claim 19, wherein said at least one bus bridge is a power-down bus bridge operable upon receipt of a power-down signal to generate a flush request signal *(Section 0031, lines 1-16 – State the following: "Referring to FIG. 9, the operation of the present invention is illustrated. The trace packets are generated and converted to export trace packets. After a halt is signaled during a non-interruptible code segment, execution of the code segment is continued until an appropriate halt point is found. The present invention, as shown in FIG. 9, stops generating trace packets. Export trace packets are generated for the trace packets that have been generated. However, when there is a remainder, the flush*

trace unit generates a flush packet that completes the data generated by the non-interruptible code segment. The flush packet will add logic "0"s to the incomplete packets. In addition, flush packets will be generated to provide sufficient logic signals to populate a standard memory location in the memory unit. When the target processor begins operation after a pause, the trace packets are converted into export trace packets as before")

- and to delay power down of said one or more trace data sources until all trace data generated by said trace data sources prior to said flush point has been output. *(Section 0033, lines 1-3 – State the following: "The present invention provides a technique for completing the transfer of trace data after the generation of halt signal for a non-interruptible code segment")*

Claim 22. A method as claimed in claim 20, wherein said data processing logic for which said one or more trace data sources generates trace data is powered down with said one or more trace data sources. *(Section 0033, lines 10-14 – State the following: "Logic "0"s complete the contents of the flush packets. In addition, flush packets are generated to insure that logic signals are available to populate the memory locations into which the packet group payloads are being entered")*

Claim 23. A method as claimed in claim 22, wherein said data processing logic and said one or more trace data sources are within a common power domain within an integrated circuit comprising a plurality of power domains. *(Section 0034, lines 1-14 – State the following, which denotes a plurality of power domains as each stream can be turned off individually. The present invention relies on the ability of relate the timing trace stream and the program counter trace stream. This relationship is provided by having periodic sync ID information transmitted in each trace stream. In addition, the timing packets are grouped in packets of eight signals identifying whether the program counter or the pipeline advanced or*

didn't advance. The sync markers in the program counter stream include both the periodic sync ID and the position in the current eight position packet when the event occurred. Thus, the clock cycle of the event can be specified. In addition, the address of the program counter is provided in the program counter sync markers so that the debug halt event can be related to the execution of the program")

Claim 24. A method as claimed in claim 14, wherein said flush signal generator operable upon receipt of a power-down signal to generate and flush request signal and to delay power down of said one or more trace data sources until all trace data generated by said trace data sources prior to said flush point has been output. *(Section 0031, lines 1-16 – State the following: "Referring to FIG. 9, the operation of the present invention is illustrated. The trace packets are generated and converted to export trace packets. After a halt is signaled during a non-interruptible code segment, execution of the code segment is continued until an appropriate halt point is found. The present invention, as shown in FIG. 9, stops generating trace packets. Export trace packets are generated for the trace packets that have been generated. However, when there is a remainder, the flush trace unit generates a flush packet that completes the data generated by the non-interruptible code segment. The flush packet will add logic "0"s to the incomplete packets. In addition, flush packets will be generated to provide sufficient logic signals to populate a standard memory location in the memory unit. When the target processor begins operation after a pause, the trace packets are converted into export trace packets as before." Section 0033, lines 1-3 – State the following: "The present invention provides a technique for completing the transfer of trace data after the generation of halt signal for a non-interruptible code segment")*

Claim 25. A method as claimed in claim 19, comprising a trace data funnel operable to combine trace data signals received from a plurality of trace data sources via respective trace data buses onto a single trace data bus.

(Sections 0023-0024 – State the following: "Referring to FIG. 3, the relationship between selected components in the target processor 20 is illustrated. The data trace generation unit 201 includes a packet assembly unit 2011 and a FIFO (first in/first out) storage unit 2012, the program counter trace generation unit 202 includes a packet assembly unit 2021 and a FIFO storage unit 2022, and the timing trace generation unit 203 includes a packet generation unit 2031 and a FIFO storage unit 2032. As the signals are applied to the packet generators 201, 202, and 203, the signals are assembled into packets of information. The packets in the preferred embodiment are 10 bits in width. Packets are assembled in the packet assembly units in response to input signals and transferred to the associated FIFO unit. The scheduler/multiplexer 204 generates a signal to a selected trace generation unit and the contents of the associated FIFO storage unit are transferred to the scheduler/multiplexer 204 for transfer to the emulation unit. Also illustrated in FIG. 3 is the sync ID generation unit 207. The sync ID generation unit 207 applies an SYNC ID signal to the packet assembly unit of each trace generation unit. The periodic signal, a counter signal in the preferred embodiment, is included in a current packet and transferred to the associated FIFO unit. The packet resulting from the SYNC ID signal in each trace is transferred to the emulation unit and then to the host processing unit. In the host processing unit, the same count in each trace stream indicates that the point at which the trace streams are synchronized. In addition, the packet assembly unit 2031 of the timing trace generation unit 203 applies and INDEX signal to the packet assembly unit 2021 of the program counter trace generation unit 202. The function of the INDEX signal will be described below. Referring to FIG. 4A, the assembly of timing packets is illustrated. The signals applied to the timing trace generation unit 203 are the CLOCK signals and the ADVANCE signals. The CLOCK signals are system clock signals to which the operation of the central processing unit 200 is

synchronized. The ADVANCE signals indicate an activity such as a pipeline advance or program counter advance (()) or a pipeline non-advance or program counter non-advance (1). An ADVANCE or NON-ADVANCE signal occurs each clock cycle. The timing packet is assembled so that the logic signal indicating ADVANCE or NON-ADVANCE is transmitted at the position of the concurrent CLOCK signal. These combined CLOCK/ADVANCE signals are divided into groups of 8 signals, assembled with two control bits in the packet assembly unit 2031, and transferred to the FIFO storage unit 2032")

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8 and 21 are rejected under 35 U.S.C.103(a) as being unpatentable over Swoboda as applied to claims 1, 6-7, 14, and 19-20 above, further in view of Humpherys et al. (US Patent 6,128,682).

Swoboda teaches the limitations of claims 1, 6-7, 14, and 19-20 for the reasons above.

Swoboda's invention differs from the claimed invention in that there is no specific reference to forcing the trace buses into a predetermined state.

Swoboda fails to teach claims 8 and 21, which state "Apparatus as claimed in claim 7 (or 20), wherein said power-down bridge bus forces said one of said one or more trace buses into a predetermined state prior to power down of said one or more trace data sources". However, Humpherys' invention discloses a "The computer system of claim 11, wherein the device

includes a bridge device adapted to drive the voltages on the second plurality of bus lines to a predetermined state in response to the predetermined voltage on the second grant line" (Column 10, lines 33-37). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Method and Apparatus for a Flush Procedure in an Interrupted Trace Stream" of Swoboda and Humpherys' "Method and Apparatus for Bus Isolation" before him at the time the invention was made, to force the buses into a predetermined state prior to power-down so that the system would be uniform, thereby running more efficiently.

6. Claims 13 and 26 are rejected under 35 U.S.C.103(a) as being unpatentable over Swoboda as applied to claims 1, 6-7, 12, 14, 19-20, and 25 above.

Swoboda teaches the limitations of claims 1, 6-7, 12, 14, 19-20, and 25 for the reasons above.

Swoboda's invention differs from the claimed invention in that there is no specific reference to the flush signal generator being part of said trace data funnel.

Swoboda fails to teach claims 13 and 26, which state "Apparatus as claimed in claim 12 (or 25), wherein said at least one flush signal generator is part of said trace data funnel". However, even though Swoboda does not explicitly include the flush signal generator as part of the trace data funnel, both components are still part of the system and perform the same necessary functions as the applicant's invention. Integrating two objects does not make an invention novel, nor does it change the functionality of the invention. Therefore, it would have obvious to one skilled in the art at the time of the "Method and Apparatus for a Flush Procedure in an Interrupted Trace Stream" of Swoboda, to include the flush signal generator as part of said

trace data funnel so that the components would be more closely connected, thereby making the system run more efficiently.

For more information, please reference In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965) (A claim to a fluid transporting vehicle was rejected as obvious over a prior art reference which differed from the prior art in claiming a brake drum integral with a clamping means, whereas the brake disc and clamp of the prior art comprise several parts rigidly secured together as a single unit. The court affirmed the rejection holding, among other reasons, "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice."); but see Schenck v. Nortron Corp., 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983) (Claims were directed to a vibratory testing machine (a hard-bearing wheel balancer) comprising a holding structure, a base structure, and a supporting means which form "a single integral and gaplessly continuous piece." Nortron argued that the invention is just making integral what had been made in four bolted pieces. The court found this argument unpersuasive and held that the claims were patentable because the prior art perceived a need for mechanisms to dampen resonance, whereas the inventor eliminated the need for dampening via the one-piece gapless support structure, showing insight that was contrary to the understandings and expectations of the art.).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100